Notice of Allowability	Application No.	Applicant(s)	_
	10/720,159	KITANI ET AL.	
	Examiner	Art Unit	
	Amare Mengistu	2629	
The MAILING DATE of this communication appearable All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in the or other appropriate communic GHTS. This application is subj	s application. If not included ation will be mailed in due course. THIS	е
1. This communication is responsive to <i>Nov.25,2003</i> .			
2. The allowed claim(s) is/are <u>1-12</u> .			
3.			
Attachment(s)  1. ☑ Notice of References Cited (PTO-892)  2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)  3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 11/25/2003  4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Sum Paper No./Ma 98), 7. ☐ Examiner's Am	il Date .	

U.S. Patent and Trademark Office PTOL-37 (Rev. 7-05)

## **DETAILED ACTION**

## **EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Remus Fetca on Thursday April 20, 2006.

The application has been amended as follows:

## In the claim:

Cancel claim 13.

## Allowable Subject Matter

- 1. Claims 1-12 are allowed.
- 2. The following is an examiner's statement of reasons for allowance: the cited prior arts (Kawase et al. and Wodnicki) has failed to teach applicants claimed invention "A bidirectional shift register comprising: an output circuit that includes a first transistor having a conductive path between a first clock terminal and an output terminal and a second transistor having a conductive path between a power supply electrode and the output terminal; an input circuit that includes a third transistor having a conductive path between a forward direction pulse input terminal and a control electrode of the first

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transistor, a fourth transistor having a conductive path between a backward direction pulse input terminal and the control electrode of the first transistor and a fifth transistor having a conductive path between the power supply electrode and a control electrode of the second transistor; a reset circuit that includes a sixth transistor having a conductive path between a second clock terminal and the control electrode of the second transistor. a seventh transistor having a conductive path between a third clock terminal and the control electrode of the second transistor and an eighth transistor having a conductive path between the power supply electrode and the control electrode of the first transistor. which makes the path between the sixth transistor, the control electrode of the second transistor and a control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the seventh transistor non-conductive in forward direction pulse shift and which makes the path between seventh transistor, the control electrode of the second transistor and the control electrode of the eighth transistor conductive as well as making the path between the fifth transistor and the sixth transistor non-conductive in backward direction pulse shift; and an inversion preventing circuit that prevents inversion of a voltage level in the control electrode of the second transistor when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off.."; and " an input circuit in which a pulse is inputted to a fifth transistor having a conductive path between a power supply electrode and a second transistor; an output circuit configured to output the clock signal inputted to the first clock terminal by a first transistor, and output a power supply voltage by the second transistor; a reset circuit

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configured to make the path between a second clock terminal and the fifth transistor conductive as well as making the path between a third clock terminal and the fifth transistor non-conductive in forward direction pulse shift, to make the path between the second clock terminal and the fifth transistor non-conductive as well as making the path between the third clock terminal and the fifth transistor conductive in backward direction pulse shift; and an inversion prevention circuit that prevents inversion of a voltage level in the control electrode of the second transistor when a voltage level of a clock signal inputted to the first clock terminal is inverted in a state where the first transistor is on and the second transistor is off. ".

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amare Mengistu whose telephone number is (571) 272-7674. The examiner can normally be reached on M-F,T-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3639. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Amare Mengistu

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4/24/06